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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,304	12/13/2001	Ravindra M. Kapre	01-721/LSI1P185	8043

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EXAMINER	
SEFER, AHMED N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/020,304	Applicant(s) RAVINDRA ET AL	
	Examiner A. Sefer	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. The amendment filed on 11/29/02 has been entered and new claims 22-26 have been added.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki US Patent No. 6,066,880 in view of Kizilyalli US Patent No. 5,767,557.

Kusunoki discloses (see figs. 68-79, col. 3, lines 5-42 and col. 7, lines 60-65) a semiconductor device or PMOS/NMOS transistor (as in claims 6 and 7) having at least an insulating gate dielectric layer 4 and a gate fabricated upon a semiconductor substrate or p-type/ n-type (as in claims 2 and 3), a buried channel 10 or p-type /n-type buried channel (as in claims 2 and 3) implanted below the insulating gate dielectric, the buried channel being doped with a predetermined do pant so that when the gate is biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer, but do

not specifically disclose a peak concentration positioned at a selected level in the substrate below the gate dielectric layer.

Kizilyalli discloses in figs. 1 and 8-10 a PMOS transistor having a buried channel 15 implanted below an insulating gate dielectric 16, the buried channel being doped with a predetermined dopant and a peak concentration positioned at a selected level in the substrate below the gate dielectric layer.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Kizilyalli with Kusunoki's device, since that would provide a reduced channel punch-through as taught by Kizilyalli.

As to claims 4 and 5, Kusunoki discloses an inversion bias from a gate to a substrate.

As to claims 8 and 9, Kusunoki discloses a MOS capacitor comprising part of a one transistor random access memory.

As to claim 22, Kizilyalli discloses (see col. 5, lines 6-19) an insulating gate dielectric layer and a substrate forming an interface and a peak concentration of implanted dopants in the buried channel located within a few hundred angstroms below the interface, which falls within the range recited in the claim.

4. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al. US Patent No. 5,998,828 in view of Kusunoki and Kizilyalli.

Ueno et al disclose (see figs. 5-8 and col. 37, lines 19-30) an integrated circuit fabricated on a semiconductor substrate and a having at least two devices, each having a different gate oxide thickness, the circuit comprising a first device T41 having a gate

disposed on a gate dielectric layer having a first thickness and a first effective gate dielectric value and disposed on the semiconductor substrate; a second device T42 having a gate disposed on a gate dielectric layer having the first thickness and the first effective gate dielectric value, the gate dielectric layer fabricated a semiconductor substrate, a buried channel implanted below the gate dielectric layer, the buried channel being doped with a predetermined dopant , wherein the effective gate dielectric of the second device is a predetermined value greater than the first effective gate dielectric value, but do not specifically disclose the dopant concentration acting as a supplemental gate dielectric layer to increase effective dielectric thickness or a peak concentration of the dopant positioned at a selected level in the substrate below the gate dielectric layer.

Kusunoki discloses (see figs. 68-79 and 42-46, col. 8, lines 4-10) a buried channel being doped with a predetermined dopant acting as a supplemental gate dielectric layer to increase effective dielectric thickness.

Kizilyalli discloses in figs. 1 and 8-10 a PMOS transistor having a buried channel 15 implanted below an insulating gate dielectric 16, the buried channel being doped with a predetermined dopant and a peak concentration positioned at a selected level in the substrate below the gate dielectric layer.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Kusunoki, so that breakdown voltage of the channel can be controlled while effective dielectric thickness is being

increased. It would have been obvious to incorporate the teachings of Kizilyalli, since that would provide a reduced channel punch-through as taught by Kizilyalli.

As to claim 24, Kizilyalli discloses (see col. 5, lines 6-19) an insulating gate dielectric layer and a substrate forming an interface and a peak concentration of implanted dopants in the buried channel located within a few hundred angstroms below the interface, which falls within the range recited in the claim.

As to claim 25, Kusunoki discloses a MOS capacitor device.

As to claim 26, Kusunoki discloses a p-type substrate and an n-type buried channel.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Fang et al US ref. 4,302,764 disclose a nondestructive read-out memory cell having a buried channel.

b. Imai US ref. 6,222,2345 discloses a circuit comprising a plurality of devices having different effective gate oxide.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
March 2, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800